REMARKS

In the Office Action dated October 7, 2005, pending Claims 1-7, 9-15, 17-19, 21 and 23-25 were examined and rejected. Claims 8, 16, 20, 22 and 26-30 were previously cancelled. In response, Claims 1, 9, 15 and 21 are amended, no claims are cancelled and no claims are added. Applicant reserves the right to prosecute the former claims in a divisional or continuation application. Applicant respectfully requests reconsideration of pending Claims 1-7, 9-15, 21 and 23-25 in view of at least the following remarks.

I. Claims Rejected Under 35 U.S.C. §103

The Examiner has rejected Claims 1-3, 10 and 11 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 4,816,815 to Yoshiba ("Yoshiba") in view of U.S. Patent No. 6,396,473 issued to Callahan et al. ("Callahan"). Applicant respectfully traverses this rejection.

Regarding Claim 1, Claim 1 is amended to recite the following claim features, which are neither taught nor suggested by Yoshiba in view of Callahan or the references of record:

> a first frame buffer divided into a plurality of regions;
> . . .; and
> a controller to identify each region of the first frame buffer including updated data and to simultaneously copy data within each identified region to both the second frame buffer and to the display monitor as the updated data within each respective, identified region is needed to refresh the display monitor, wherein at least one identified region includes both an updated portion of data and an unupdated portion of data. (Emphasis added.)

In response to Applicant's arguments for amended Claim 1, the Examiner has indicated that the features of amended Claim 1 are taught by col. 2, lines 47-67 of Yoshiba. (*See*, pg. 2, ¶3 of the Office Action mailed October 7, 2005.) As indicated by the Examiner:

> Applicant's attention is drawn to Yoshiba col. 2, lines 40-67 wherein "the identifying" takes place " . . . the control is constructed to control the first and second memories . . . and a command from the host machine specifying that part of display data stored in the first memory which has been updated . . . display data in the updated part is transferred from the first memory to the display unit to be displayed thereon and to the second memory to be stored therein . . . lines 40-48". Therefore, Yoshiba discloses "identifying process" similar to the amended Claim 1. (pg. 2, ¶3 of the Office Action mailed October 7, 2005.)

Applicant respectfully submits that the portion of text of Yoshiba referred to by the Examiner (col. 2, lines 40-67) refers to the second embodiment of Yoshiba. As described below, Yoshiba indicates that according to the second embodiment:

> Only the display data in the particular region 420 which the CPU 20 updated is read out of the VRAM 16 and displayed on the CRT 10 and at the same time, its copy is reproduced in the VRAM 24. (col. 10, lines 5-11.) (Emphasis added.)

In contrast to the explicit disclosure from the above-recited passage of Yoshiba, Claim 1 recites a controller to identify each region of the first frame buffer, including updated data, and the copying of the data within each identified region to both the second frame buffer and the display monitor, wherein at least one identified region includes both an updated portion of data and an unupdated portion of data.

Hence, in contrast to the above-recited features of amended Claim 1, Yoshiba describes refreshing of a CRT with updated display data with reference to FIGS. 8 and 14. As described within Yoshiba:

> Assume that the CPU 20, as shown in FIG. 8, has updated only limited part of one frame, i.e., hatched part 314. Specifically, let it be assumed that the CPU 20 has updated video data over a certain region 314 whose area is an integral multiple of one horizontal scanning line in the frame, while maintaining the other regions 316*a* and 316*b* unchanged.
>
> Then, the first embodiment would transfer one frame of display data from the VRAM 16 to the CRT 10 and VRAM 24 despite the partial change of the display data, that is, it would develop a copy of one frame of display data in the VRAM 24 despite the partial change of the display data. In contrast, in accordance with the second embodiment, only the region 314 updated anew is transferred. (col. 7, line 62 - col. 8, line 8.) (Emphasis added.)

As explicitly recited by Yoshiba regarding the second embodiment:

> As seen from the foregoing description, addresses are compared also in the horizontal direction of the picture frame so that only the display data in the particular region 420 which the CPU 20 updated is read out of the VRAM 16 and displayed on the CRT 10 and, at the same time, its copy is reproduced in the VRAM 24. (col. 10, lines 5-11.) (Emphasis added.)

Based on the above-cited passages, Applicant respectfully submits that the disclosure in Yoshiba is expressly limited to a first embodiment in which an entire frame of display data is transferred from VRAM 16 to CRT 10 and VRAM 14 despite the partial change of the display data (*see*, col. 8, lines 1-3), and a second embodiment in which the transfer of data from VRAM 16 to CRT 10 and VRAM 24 is expressly limited to only the updated display data. (*See*, col. 10,

lines 5-11.) Hence, the first embodiment referred to Yoshiba copies an entire frame despite a partial change of the display data, whereas the second embodiment expressly limits the transfer data to only such data, which has been updated, to comply with the following explicitly stated goal of Yoshiba:

> access by the CPU 20 to the VRAM 16 is inhibited only for a period wherein display data are sequentially read out of the region 314 of the VRAM 16 and transferred to the CRT 10. This offers the CPU a longer period of time within which it can make access to the VRAM 16 than in the case of the first embodiment. (*See*, col. 9, lines 36-42.) (Emphasis added.)

The teachings of Yoshiba are expressly limited to copying either an entire frame buffer, including a portion of updated data, or only the updated data. (*See*, col. 7, line 6 – col. 8, line 8.) Conversely, as recited by Claim 1, the first frame buffer is divided into a plurality of regions, one or more of which may contain a portion of updated data. As further recited by amended Claim 1, each region including update data is identified by the controller, wherein at least one identified region includes both an updated portion of data and an unupdated portion of data. Consequently, as recited by amended Claim 1, such regions are simultaneously copied to both the second frame buffer and the display monitor, regardless of whether they are entirely comprised of updated data or only contain a portion of updated data.

Hence, Applicant respectfully submits that Yoshiba fails to either teach or suggest the identification of each region from a plurality of regions of a first frame buffer that includes updated data, wherein at least one identified region includes both an updated portion of data and an unupdated portion of data, as recited by amended Claim 1. Consequently, Yoshiba cannot teach simultaneous copying of such an identified region, as recited by Claim 1.

As correctly noted by the Examiner, Yoshiba is silent about a first frame buffer being divided into a plurality of regions. As a result, the Examiner cites Callahan. However, in contrast to the display memory control system, as disclosed by Yoshiba, or the scan synchronized dual frame buffer graphics system, as recited by amended Claim 1, Callahan is directed to a memory management and buffer organization technique for preserving memory and pixel processor bandwidth while processing overlay graphic images for display on a monitor. (*See*, col. 1, lines 7–10.)

Furthermore, in contrast to the above-recited features of amended Claim 1, as explicitly disclosed by Callahan:

> Only those pixels affected by change between successive fields need to be stored in variable-size tile buffer 22 [sic] and processed by graphic processor 20. (col. 12, lines 14-17.) (Emphasis added.)

Specifically, as disclosed by Callahan:

> Those of skill in the art also will appreciate that tile buffer 24 is of variable size and is a region or regions of physical memory allocated by tile buffer control 26. Tile buffer control 26 may, for example, include a memory management unit (MMU) suitably programmed to allocate tiles as required by tile buffer 24 and to de-allocate tiles as they are no longer needed by tile buffer 24 because of a change in the overlay graphic window requiring that more or fewer tiles be allocated. (col. 9, lines 10-18.) (Emphasis added.)

Based on the cited passages above, the disclosure in Callahan neither teaches nor suggests a first frame buffer divided into a plurality of regions, as recited by amended Claim 1. In contrast, as explicitly indicated by the cited passages above, the tile buffer 24, as disclosed by Callahan, is of variable size to enable allocation and de-allocation of tiles as they are needed due to changes in the overlay graphics window requiring that more or fewer tiles be allocated. (*See*, supra.)

Furthermore, as indicated by the cited passage above, only those pixels affected by change between successive fields need to be stored in variable size tile buffer. (*See*, col. 12, lines 14-16.) Accordingly, Applicant respectfully submits that the disclosure in Callahan is expressly limited to a variable sized tile buffer, which allocates and de-allocates tiles as they are needed, such that only pixels affected by change between successive fields need to be stored in the variable sized tile buffer.

Consequently, Applicant respectfully submits that the combination of Yoshiba in view of Callahan would fail to disclose a controller to identify at least one region of the first frame buffer, including updated data since, as disclosed by Callahan, only those pixels affected by change between successive fields need be stored in variable sized tile buffer. (*See*, col. 12, lines 14-16.)

As established by case law, a *prima facie* case of obviousness of a claimed invention requires that all claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 590 (CCP 1974). Here, Applicant respectfully submits that the limitation of Callahan in requiring that only updated pixel data be contained within tile buffer 24 (*see*, col. 12, lines 14-17) prohibits the Examiner from establishing a controller, as recited by amended Claim 1, to identify each region from a plurality of regions of a first frame buffer, which contain updated data, wherein at least one identified region includes both an updated portion of data and

an unupdated portion of data, since according to Callahan, all tiles within the tile buffer 24, as taught by Callahan, are required to contain updated data and once processed, are de-allocated. (*See*, supra.)

Accordingly, Applicant respectfully submits that the Examiner fails to establish a *prima facie* case of obviousness of amended Claim 1, since the combination of Yoshiba in view of Callahan fails to either teach or suggest each of the recited features of amended Claim 1. In re Royka, supra.

Furthermore, the Federal Circuit Court of Appeals in In re Rijckaert, 9 F.3d 1531, 28 U.S.P.Q. 2d 1955 (Fed. Cir. 1993) held that:

> In rejecting claims under 35 U.S.C. § 103, the examiner bears the initial burden of presenting a *prima facie* case of obviousness. . . . "A *prima facie* case of obviousness is established when the teaching from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art.". . . If the examiner fails to establish a *prima facie* case, the rejection is improper and will be overturned. (Emphasis added.) 9 F.3d at 1532, 28 U.S.P.Q. 2d at 1956.

Here, Applicant respectfully submits that Callahan is directed to a memory management and buffer organization technique for preserving memory and pixel processor bandwidth while processing overlay graphics images for display on a monitor. (*See*, col. 1, lines 7-10.) Applicant respectfully submits that the handling of overlay images is distinct from the display memory control system, as disclosed by Yoshiba, as well as the scan synchronized dual-frame buffer graphics system, as recited by amended Claim 1. Hence, Applicant respectfully submits that the disclosure in Callahan represents non-analogous art.

Applicant respectfully submits that the combined teachings of Yoshiba in view of Callahan would not have suggested the claimed subject to one of ordinary skill in the art, since the memory management for overlay images, as disclosed in Callahan, represents analogous art, the teachings of which are not applicable to graphics display systems, for example, as disclosed by amended Claim 1 and Yoshiba. Accordingly, Applicant respectfully submits that the combined teachings of Yoshiba in view of Callahan would not have suggested the claimed subject matter to one of ordinary skill in the art, as required to establish a *prima facie* case of anticipation. Id.

Consequently, for at least the reasons described above, Applicant respectfully submits that Claim 1, as amended, is patentable over the combination of Yoshiba in view of Callahan, as well as the references of record. Id. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of amended Claim 1.

Regarding Claims 2 and 3, Claims 2 and 3, based on their dependency from Claim 1, and for at least the reasons described above, are also patentable over the combination of Yoshiba in view of Callahan. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of amended Claims 2 and 3.

The Examiner has rejected Claims 4-6, 12-15, 17-19, 21 and 23-25 under 35 U.S.C. §103(a) as being unpatentable over Yoshiba in view of Callahan as applied to Claim 1 and further in view of U.S. Patent No. 5,757,364 to Ozawa et al. ("Ozawa"). Applicant respectfully traverses this rejection.

Regarding Claims 4-6, Claims 4-6 depend from Claim 1. Regarding the Examiner's citing of Ozawa, Applicant respectfully submits that the Examiner citing of Ozawa fails to rectify the deficiencies of the combination of Yoshiba in view of Callahan to either teach or suggest a controller to identify each region from a plurality of regions of a first frame buffer that includes updated data and to simultaneously copy data within each region to both a second frame buffer and a display monitor, wherein at least one identified region includes both an updated portion of data and an unupdated portion of data, as recited by amended Claim 1. Accordingly, for at least the reasons described above, Applicant respectfully submits that Claim 1, as amended, is patentable over the combination of Yoshiba in view of Callahan and further in view of Ozawa.

Consequently, Claims 4-6, based on their dependency from Claim 1, and for at least the reasons described above, are also patentable over the combination of Yoshiba in view of Callahan and further in view of Ozawa. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of amended Claims 4-6.

Regarding Claims 15 and 21, Claims 15 and 21 recite the following claim feature, which is neither disclosed nor suggested by the combination of Yoshiba in view of Callahan and further in view of Ozawa:

> identifying, within a first frame buffer memory divided into a plurality of regions, each region including updated data; and
> simultaneously copying data within each identified region of the first frame buffer memory to both the second frame buffer memory and to a display

monitor as the data within each respective, identified region is needed to refresh the display monitor, wherein at least one identified region includes both an updated portion of data and an unupdated portion of data. (Emphasis added.)

Applicant respectfully submits that the above-described and recited features of amended Claims 15 and 21 are analogous to the features of amended Claim 1. Hence, Applicant's arguments regarding amended Claim 1 apply to the Examiner's rejection of Claims 15 and 21, as obvious in view of the combination of Yoshiba in view of Callahan and further in view of Ozawa.

As indicated above, the combination of Yoshiba in view of Callahan could not teach the identification of each region, including updated data, from a plurality of regions of a first frame buffer, wherein at least one identified region includes both an updated portion of data and an unupdated portion of data since, as explicitly recited by Callahan, only those pixels affected by change between successive fields need to be stored in variable sized tile buffer. (*See*, col. 12, lines 14-16.) Hence, since Callahan expressly limits tile buffer 24 to contain only updated pixel data, the combination of Yoshiba in view of Callahan would fail to teach identification of one of such tiles within tile buffer 24, which contain , wherein at least one identified region includes both an updated portion of data and an unupdated portion of data, since all data within tile buffer is required to contain updated data. (*See*, supra.)

Accordingly, Applicant respectfully submits that the combination of Yoshiba in view of Callahan and further in view of Ozawa would not have suggested the claimed subject matter, as recited by independent Claims 15 and 21, as required to establish a *prima facie* case of anticipation. In re Rijckaert, supra.

Consequently, Applicant respectfully submits that Claims 15 and 21 are both patentable over the combination of Yoshiba in view of Callahan and further in view of Ozawa. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 15 and 21.

Regarding Claims 17-19, Claims 17-19, based on their dependency from Claim 15, and for at least the reasons described above, are also patentable over the combination of Yoshiba in view of Callahan and further in view of Ozawa. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 17-19.

Regarding Claims 23-25, Claims 23-25, based on their dependency from Claim 21, and for at least the reasons described above, are also patentable over the combination of Yoshiba in view of Callahan and further in view of Ozawa. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 23-25.

The Examiner has rejected Claims 7 and 9 under 35 U.S.C. §103(a) as being unpatentable over Yoshiba in view of Callahan, as applied to Claim 1, and further in view of U.S. Patent No. 5,790,138 to Hsu ("Hsu"). Applicant respectfully traverses this rejection.

Regarding Claim 7, Claim 7 depends from Claim 1. Regarding the Examiner's citing of Hsu, Applicant respectfully submits that the Examiner's citing of Hsu fails to rectify the deficiencies of Yoshiba in view of Callahan to teach a controller, which identifies each region from a plurality of regions of a first frame buffer that includes updated data. Hence, the Examiner is prohibited from establishing a *prima facie* case of obviousness of amended Claim 1, since the prior art combination of Yoshiba in view of Callahan and further in view of Hsu fails to teach or suggest all claim features recited by amended Claim 1. In re Royka, supra. Consequently, Applicant respectfully submits that amended Claim 1 is patentable over the combination of Yoshiba in view of Callahan and further in view of Hsu.

Accordingly, Claim 7, based on its dependency from Claim 1, and for at least the reasons described above, is patentable over the combination of Yoshiba in view of Callahan and further in view of Hsu. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claim 7.

Regarding Claim 9, Claim 9 recites an analogous claim feature to Claim 1, which is neither disclosed nor suggested by the combination of Yoshiba in view of Callahan and further in view of Hsu:

> a controller to identify each region of the primary frame buffer memory including updated pixel data and simultaneously copy pixel data within each identified region to both the secondary frame buffer memory and to the display monitor as the pixel data within each respective, identified region is needed to refresh the display monitor, wherein at least one identified region includes both an updated portion of data and an unupdated portion of data. (Emphasis added.)

Applicant respectfully submits that the above-recited controller is analogous to the controller recited by amended Claim 1. Hence, Applicant's arguments regarding amended Claim 1 apply to the Examiner's rejection of Claim 9 as obvious under 35 U.S.C. §103(a) over Yoshiba

in view of Callahan and further in view of Hsu. Accordingly, for at least the reasons described above, Applicant respectfully submits that Claim 9, as amended, is patentable over the combination of Yoshiba in view of Callahan and further in view of Hsu. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of amended Claim 9.

Regarding Claims 10-13, Claims 10-13, based on their dependency from Claim 9, and for at least the reasons described above, are also patentable over the combination of Yoshiba in view of Callahan and further in view of Hsu. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 10-14.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: January 9, 2006

By: _____
Joseph Lutz, Reg. No. 43,765

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

CERTIFICATE OF MAILING:
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on January 9, 2006

_____
Marilyn Bass January 9, 2006